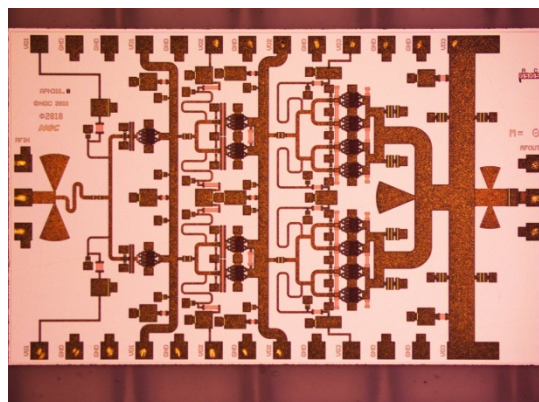


APN318

47.2-51.4 GHz

GaN Power Amplifier

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X = 3.2mm Y = 2.0mm

Product Features

- RF frequency: 47.2 to 51.4 GHz
- Linear Gain: 12-16 dB across the band
- Psat: 8 Watt on wafer
- Psat: 3.2 Watt (CW)
- Die Size: 6.4 mm²
- 0.15um GaN HEMT Process
- 3 mil SiC substrate
- DC Power: 28 VDC @ 1.62 A

Export Information

ECCN: **5A991.g**

HTS (Schedule B) code: **8542.33.0000**

Applications

- 5G Wireless
- Internet of Things (IoT)
- SatCom Terminals

Product Description

The APN318 GaN HEMT Power/Driver amplifier is a three-stage Single-ended power device, designed for use in 5G wireless and SatCom Terminals. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

Specification *	Min	Typ	Max	Unit
Frequency	47.2		51.4	GHz
Linear Gain	12	13.5	16	dB
Input Return Loss	-30	-12		dB
Output Return Loss	-25	-12	-11.5	dB
Psat (PP*)	27.5**		39	dBm
PAE @ Psat (PP*)		11.5		%
Max PAE (PP*)		13		%
Psat (CW)		35		dBm
PAE (CW)		4		%
Max PAE (CW)		6		%
Vd1=Vd1a=Vd2=Vd2a=Vd3=Vd3a	20	24	28	V
Vg1, Vg1a, Vg2, Vg2a, Vg3, Vg3a		-3.5		V
Id1+Id1a		220		mA
Id2+Id2a		440		mA
Id3+Id3a		960		mA

* Pulsed-Power On-Wafer

** PIN=13 dB instead of 26 dB

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12/2/2020

Web: <http://www.as.northropgrumman.com/mps>

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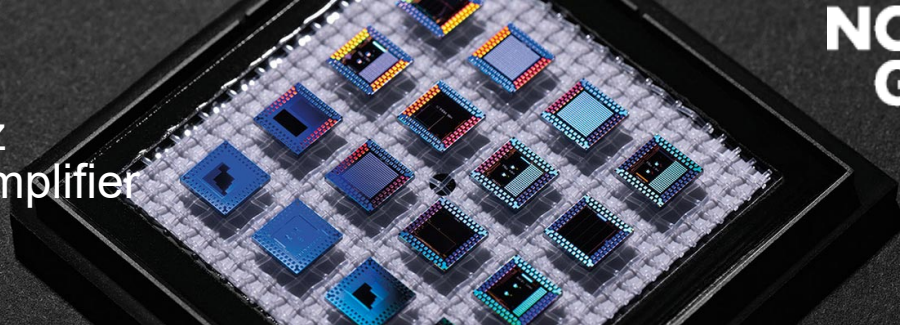
Page 1

APN318

47.2-51.4 GHz

GaN Power Amplifier

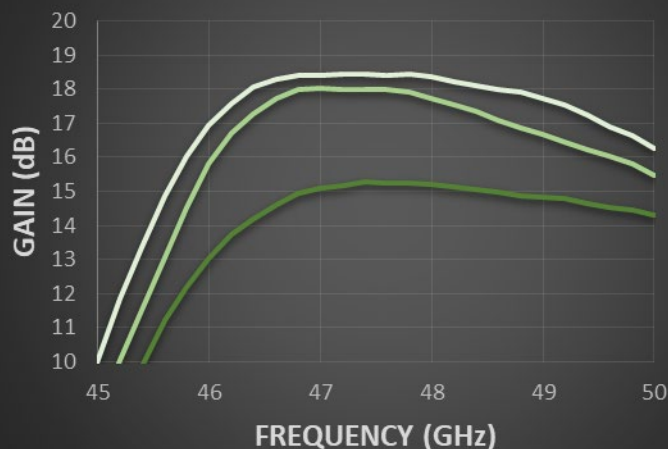
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On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 220 mA, Id2 + Id2a = 440 mA, Id3 + Id3a = 960mA

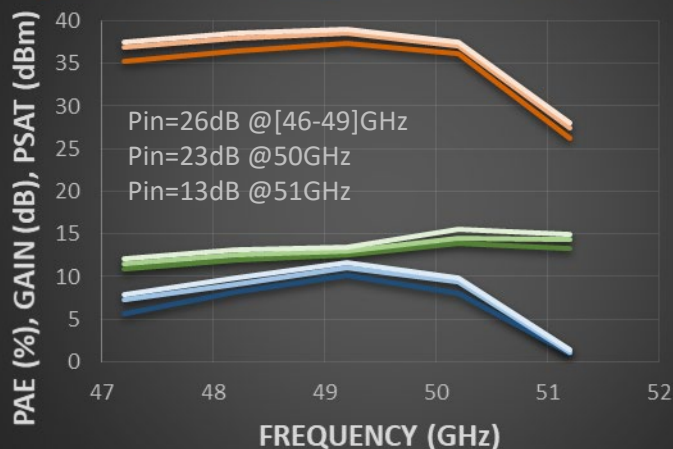
GAIN vs. Frequency

— 25 percentile — 50 percentile — 75 percentile



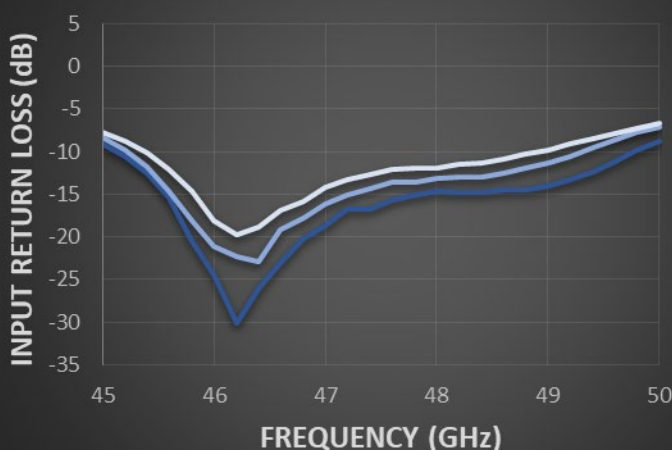
PAE, GAIN, PSAT vs. Frequency **

— PAE 25 percentile — PAE 50 percentile — PAE 75 percentile
 — Gain 25 percentile — Gain 50 percentile — Gain 75 percentile
 — Psat 25 percentile — Psat 50 percentile — Psat 75 percentile



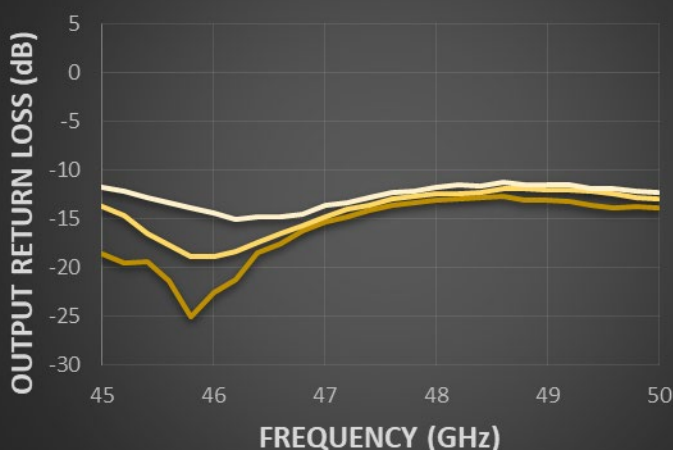
Input Return Loss vs. Frequency

— 25 percentile — 50 percentile — 75 percentile



Output Return Loss vs. Frequency

— 25 percentile — 50 percentile — 75 percentile



*Gain: is limited by the frequency measurement capabilities

**Pin=26dB @[47-49]GHz; Pin=23dB @50GHz; Pin=13dB @51GHz

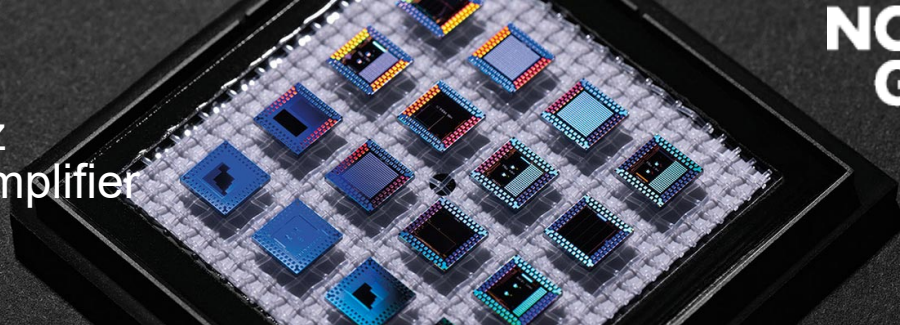
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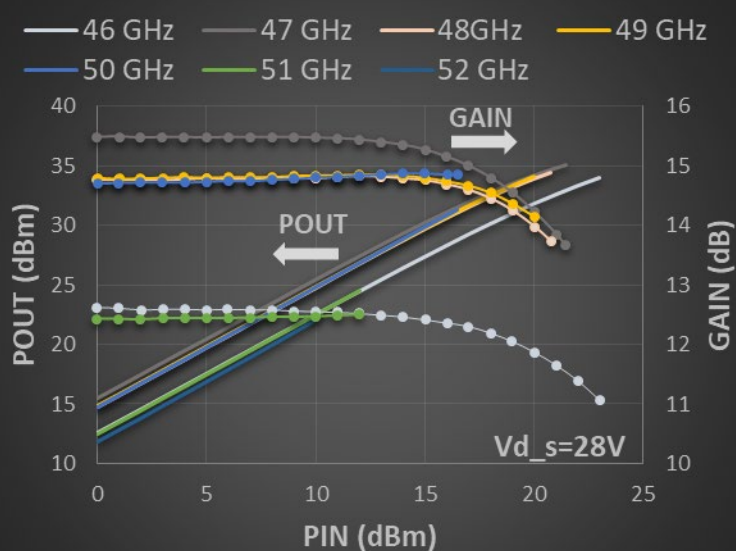
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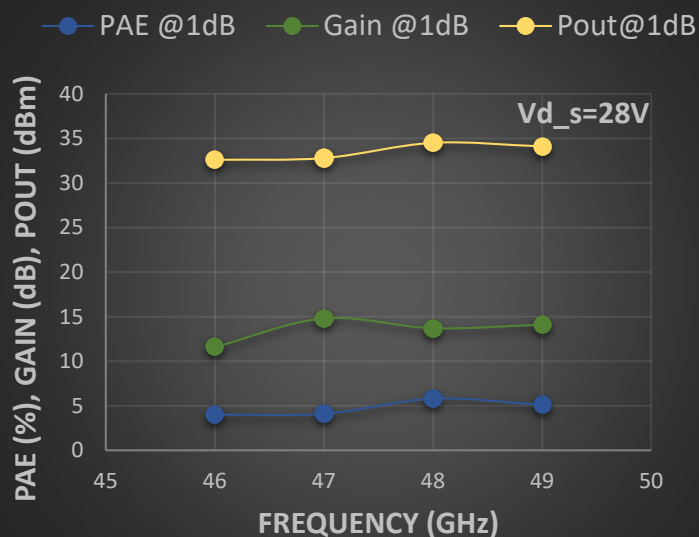
Fixture measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 28.0\text{ V}$, $I_{d1} + I_{d1a} = 220\text{ mA}$, $I_{d2} + I_{d2a} = 440\text{ mA}$, $I_{d3} + I_{d3a} = 960\text{ mA}$

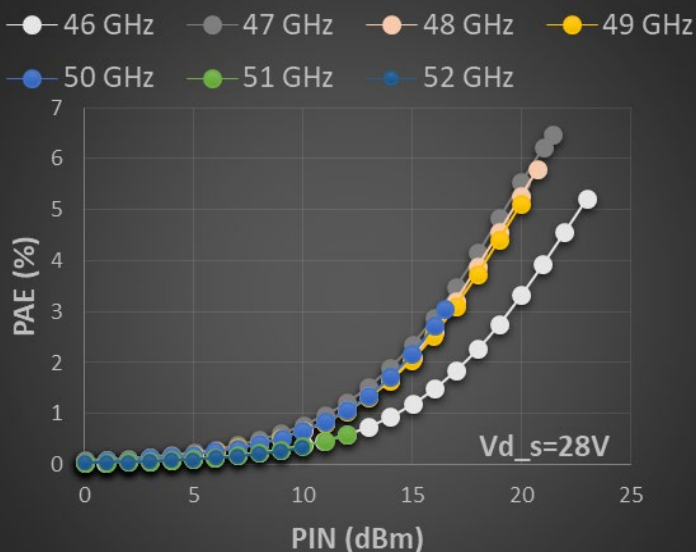
POUT and GAIN vs. PIN



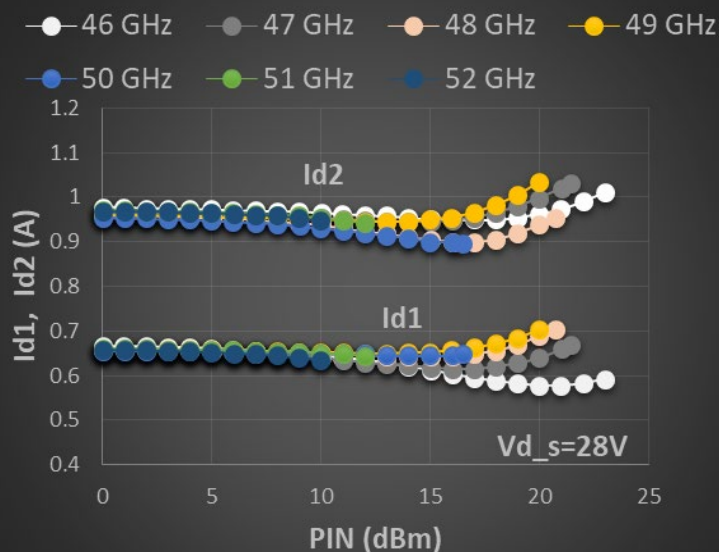
PAE, GAIN, POUT vs. FREQUENCY



PAE vs PIN



I_{d1} , I_{d2} vs PIN



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GaN Power Amplifier

Die Size and Bond Pad Locations (Not to Scale)

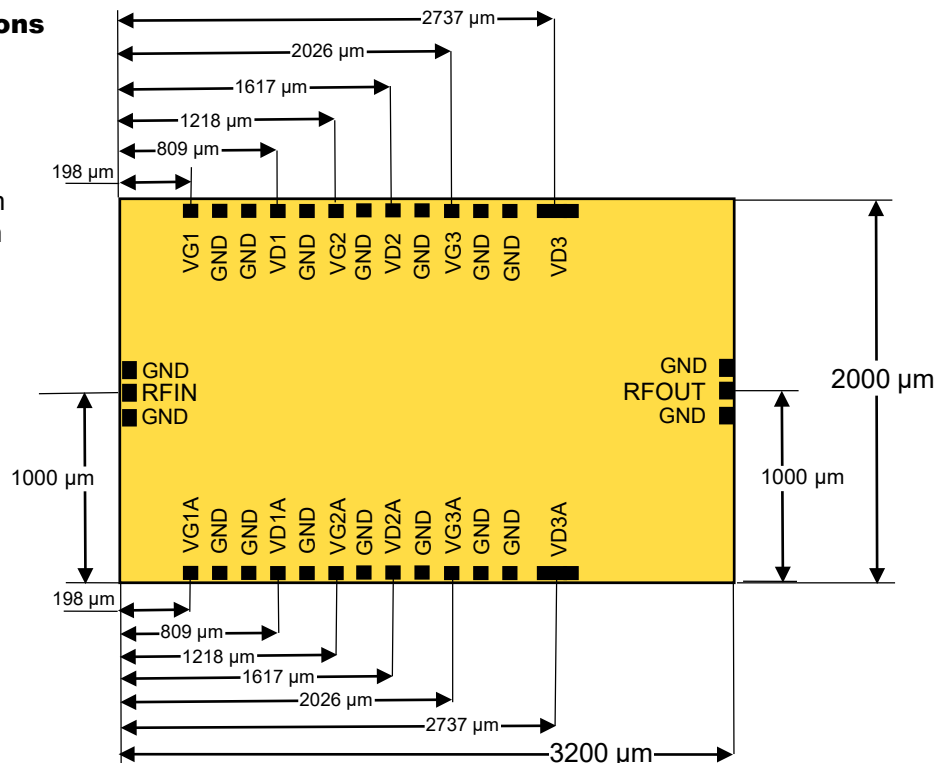
X = $3200 \mu\text{m} \pm 25 \mu\text{m}$

Y = $2000 \pm 25 \mu\text{m}$

DC Bond Pad = $100 \times 100 \pm 0.5 \mu\text{m}$

RF Bond Pad = $100 \times 100 \pm 0.5 \mu\text{m}$

Chip Thickness = $101 \pm 5 \mu\text{m}$



Biasing/De-Biasing Details:

Bias for 1st must be from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

- Limit positive gate bias (G-S or G-D) to < 1V
- Know your devices' breakdown voltages
- Use a power supply with both voltage and current limit.
- With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
 - Apply negative gate voltage (-5 V) to ensure that all devices are off
 - Ramp up drain bias to ~10 V
 - Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
 - Ramp up drain to operating bias
 - Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
- To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
 - Gradually decrease drain bias to 0 V.
 - Gradually decrease gate bias to 0 V.
 - Turn off supply voltages

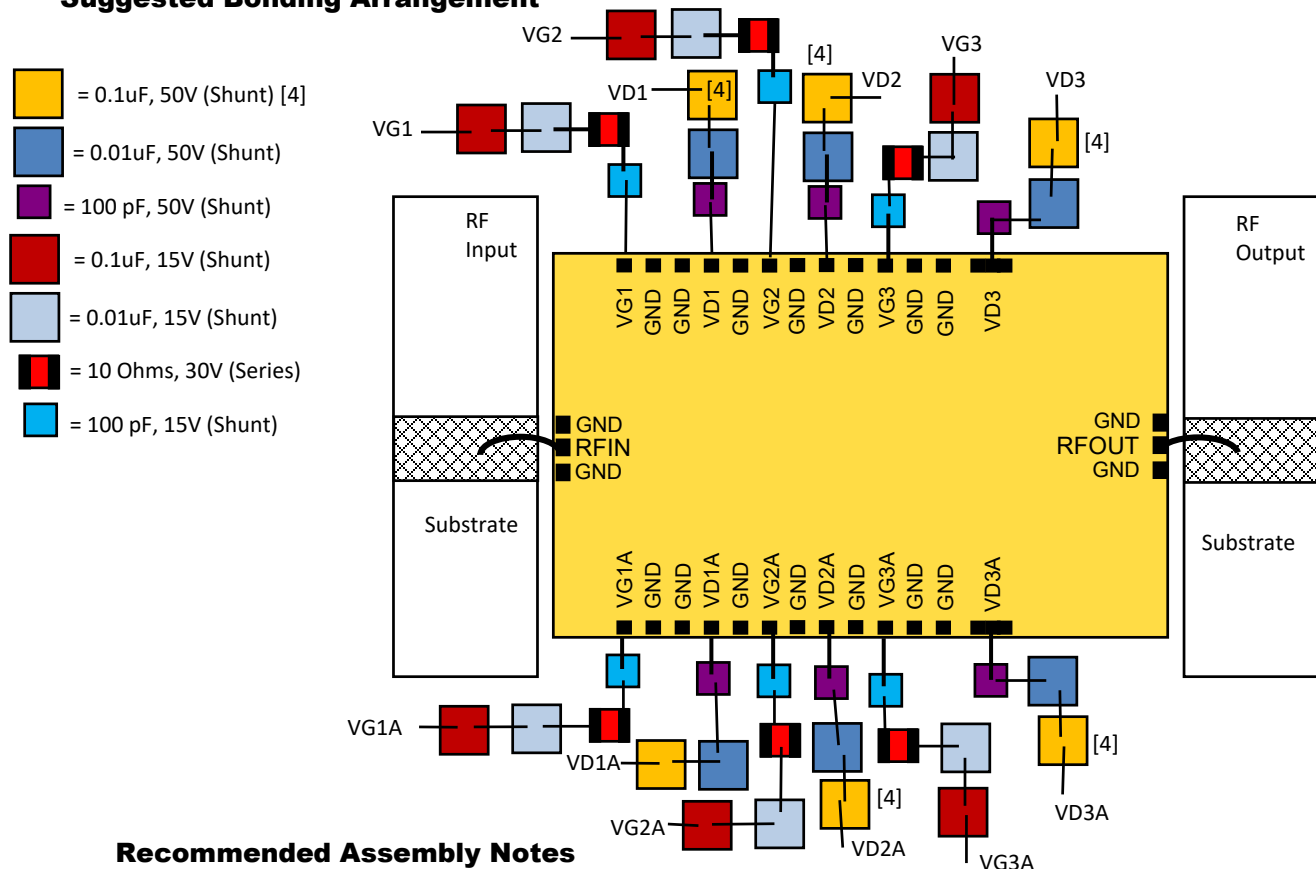
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GaN Power Amplifier

Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF, 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS. **PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!**

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